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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, SHIN HON	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 09/995,308	**Applicant(s)** DUCHARME, PAUL	
	Examiner Shin-Hon Chen	**Art Unit** 2131	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 24 March 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1,17-22, 24-33 and 41*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☒ Other: See attachment

4/12/06

CHRISTOPHER REVAK
PRIMARY EXAMINER

DETAILED ACTION

1. Claims 1, 17-22, 24-33, and 41 have been examined.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 33, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easter et al. U.S. Pat. No. 5563950 (hereinafter Easter) in view of Van Oorschot et al. U.S. Pat. No. 5850443 (hereinafter Van Oorschot).

4. As per claim 1, Easter discloses monolithic semiconductor device comprising: a memory location having an output port coupled to the input port, wherein a data value to be stored in said memory location is observable only internally to the monolithic semiconductor device (Easter: figure 2 and column 4 lines 49-65 and column 2 lines 62-64); an asymmetrical encryption engine having an input port coupled to the output port of the memory location and an output port to provide a symmetrical encryption key based on the data value (Easter: figure 5 and column 8 lines 18-26); and a symmetrical encryption engine having an input port coupled to an output port of the asymmetrical encryption engine, wherein the symmetrical encryption engine is to perform an encryption function using the symmetrical encryption key (Easter: figure 5 and column 8 lines

18-26); wherein at least one silicon die pad having an input coupled to the output port of said memory location to provide temporary access to said memory location (Easter: column 8 lines 18-26). In addition, Van Oorschot discloses that the asymmetrical encryption key is output to symmetrical encryption engine (Van Oorschot: column 5 lines 39-59). It would have been obvious to one having ordinary skill in the art to allow one encryption engine to provide key information to the other encryption engine either directly or indirectly. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Van Oorschot within the system of Easter because it provides multiple layers of encryption/decryption to secure data being transferred.

5. As per claim 33, Easter discloses a method comprising the steps of: accessing, by a first encryption engine internal to a monolithic semiconductor device, data from a memory location internal to the monolithic semiconductor device, wherein the memory location is accessible only internal to the monolithic semiconductor device (Easter: figure 5 and column 8 lines 18-26); generating, at the first encryption engine, a first encryption key based on the data from the memory location wherein the data represents a second encryption key (Easter: figure 5 and column 5 lines 24-36) generating the first encryption key; and providing the first encryption key for storage in the memory location (Easter: figure 5 and column 8 lines 18-26); providing the first encryption key to a second encryption engine internal to the monolithic semiconductor device (Easter: figure 5 and column 8 lines 18-26); and performing an encryption function at the second encryption engine using the first encryption key (Easter: figure 2 and column 4 lines 49-65 and column 2 lines 62-64). In addition, Van Oorschot discloses that the asymmetrical

encryption key is output to symmetrical encryption engine (Van Oorschot: column 5 lines 39-59). It would have been obvious to one having ordinary skill in the art to allow one encryption engine to provide key information to the other encryption engine either directly or indirectly. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Van Oorschot within the system of Easter because it provides multiple layers of encryption/decryption to secure data being transferred.

6. As per claim 41, claim 41 encompasses the same scope as claim 13. Therefore, claim 41 is rejected based on the same reason as in claim 13.

7. Claims 17-19, 21, 22, and 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Van Oorschot and further in view of Pitts U.S. Pub. No. 20020145931 (hereinafter Pitts).

8. As per claim 17, Easter discloses a monolithic semiconductor device comprising: an external data port having an input and an output; a first encryption engine having an input coupled to the input of said external data port and an output (Easter: figure 5 and column 8 lines 18-26); and a second encryption engine having an input coupled to the input of said external data port and an output (Easter: figure 5 and column 8 lines 18-26); a memory location having an output coupled to the input of said first encryption engine (Easter: figure 5 and column 8 lines 18-26); and wherein the first encryption engine is to provide a first encryption key based on a value stored at said memory location to said second encryption engine (Easter: figure 5 and

column 8 lines 18-26). In addition, Van Oorschot discloses that the asymmetrical encryption key is output to symmetrical encryption engine (Van Oorschot: column 5 lines 39-59). It would have been obvious to one having ordinary skill in the art to allow one encryption engine to provide key information to the other encryption engine either directly or indirectly. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Van Oorschot within the system of Easter because it provides multiple layers of encryption/decryption to secure data being transferred. Easter as modified does not explicitly disclose an isolation portion coupled to the output of said memory location and to the input of said external data port, wherein said isolation portion is modifiable to permanently prevent access of said memory location by the external data port. However, Pitts discloses an isolation fuse element that enforces one time programming of the memory (Pitts: [0011]: the fuse element and figure 1:104). It would have been obvious to one having ordinary skill in the art at the time of applicant's invention to include a fuse element in the semiconductor device because semiconductor device with fuse is well known in the art. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the teachings of Pitts within the system of Easter because it prevents external access to the memory location after data has been successfully stored into secure memory array.

9. As per claim 18, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said memory location includes non-volatile memory (Easter: column 4 lines 57-65).

10. As per claim 19, Easter as modified discloses the device as in claim 18. Easter further discloses wherein said value stored in said memory location is defined during a manufacture of the monolithic semiconductor device (Easter: column 3 lines 54-64).

11. As per claim 21, Easter as modified discloses the device as in claim 19. Easter further discloses said value is defined using a laser etching technique (Easter: column 6 lines 5-13).

12. As per claim 22, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said memory location includes volatile memory (Easter: column 4 lines 57-65).

13. As per claim 24, Easter as modified discloses the device as in claim 17. Easter further discloses wherein sad memory location is located in a specific location of the monolithic semiconductor device (Easter: figure 2).

14. As per claim 25, Easter as modified discloses the device as in claim 17. Easter further discloses wherein said value includes second encryption key (Easter: figure 5 and column 8 lines 18-26).

15. As per claim 26, Easter as modified discloses the device as in claim 25. Easter further discloses wherein said memory location is to store a plurality of encryption keys (Easter: figure 2 and column 4 lines 50-65).

16. As per claim 27, Easter as modified discloses the device as in claim 25. Easter further discloses wherein first encryption engine is to use a portion of the first encryption key to perform an encryption function (Easter: figure 5 and column 8 lines 18-40: the fuse array contains private key).

17. As per claim 28, Easter as modified discloses the device as in claim 25. Easter as modified further discloses wherein the first encryption key includes a symmetrical encryption key, and wherein said first encryption engine is an asymmetrical encryption engine and said second encryption engine is a symmetrical encryption engine (Easter: figure 5 and column 8 lines 18-26; Van Oorschot: column 5 lines 39-59).

18. As per claim 29, Easter as modified discloses the device as in claim 28. Easter as modified further discloses wherein said first encryption engine is to provide a symmetrical encryption key to said second encryption engine, and wherein said second encryption key is to perform an encryption function using the symmetrical encryption key (Van Oorschot: column 5 lines 39-59).

19. As per claim 30, Easter as modified discloses the device as in claim 17. Easter as modified further discloses wherein said isolation portion includes a fuse coupled between the input of said external port and the output of said memory location (Pitts: Pitts: [0011]: the fuse element and figure 1: 104).

20. As per claim 31, Easter as modified discloses the device as in claim 17. Easter as modified further discloses the device comprising: at least one silicon die pad having an input coupled to the output of said memory location to provide a temporary access to said memory location (Easter: figure 2 and column 4 lines 50-65).

21. As per claim 32, Easter as modified discloses the monolithic semiconductor device as in claim 1. Easter further discloses the device comprising an unique ID register coupled to the input of said encryption engine to store an unique ID (Easter: column 5 lines 27-36 and figure 3).

22. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Easter in view of Van Oorschot and further in view of Pitts and further in view of Loh et al. U.S. Pub. No. 20030093661 (hereinafter Loh).

23. As per claim 20, Easter as modified discloses the device as in claim 19. Easter as modified does not explicitly disclose wherein said value is defined using a lithographic technique. However, Loh discloses that limitation (Loh: [0003]:use of lithography). It would have been obvious to one having ordinary skill in the art to define value of the memory location using lithographic technique because lithography is one of the most common technique for hardwired programming of the ROM on semiconductor. Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant's invention to combine the

teachings of Loh within the combination of Easter-Pitts because lithography is well known technique in semiconductor industry.

Response to Arguments

24. Applicant's arguments filed 3/24/06 have been fully considered but they are not persuasive.

Regarding applicant's remarks, applicant argues that the amended independent claim discloses a silicon die pad having input coupled to the output of said memory location to provide temporary access to said memory location. However, Easter discloses that an IC chip that includes memory locations (fuse array/key array) and the public key engine is used to generate the key required by DES engine and the key is stored in key array (Figure 5, column 8 lines 18-26). Furthermore, the key array is the temporary storage area that takes output of the RSA engine and the integrated circuits are well known in the art to contain die pads. Therefore, applicant's argument is respectfully traversed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shin-Hon Chen whose telephone number is (571) 272-3789. The examiner can normally be reached on Monday through Friday 8:30am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shin-Hon Chen
Examiner
Art Unit 2131

SC

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4/12/06